CLAIMS

What is claimed is:

1. A ripple counter circuit, comprising:

a clock input terminal;

a control circuit having a test enable input terminal, a clock input terminal coupled to the clock input terminal of the ripple counter circuit, and a control output terminal, wherein the control circuit controls a signal on the control output terminal to alternate between a first value and a second value;

a first stage, comprising a first storage element having a data input terminal, a true data output terminal, a complement data output terminal, an initialization terminal, and a clock terminal, wherein the clock terminal is coupled to the clock input terminal of the ripple counter circuit, and wherein the complement data output terminal is coupled to the data input terminal; and

a plurality of additional stages, each additional stage comprising

an additional storage element having a data input terminal, a true data output terminal, a complement data output terminal, an initialization terminal, and a clock terminal, wherein the initialization terminal is coupled to the initialization terminal of the first storage element, and wherein the complement data output terminal is coupled to the data input terminal, and

an additional multiplexer having an output terminal coupled to the clock terminal of the additional storage element, a first input terminal coupled to the true data output terminal of the storage element in a preceding stage, a second input terminal coupled to the complement data output terminal of the additional storage element in the preceding stage, and a select input terminal coupled to the control output terminal of the control circuit.

2. The ripple counter circuit of Claim 1, wherein each of the first and the additional storage elements comprises a flip-flop having a true data output terminal and an inverting element coupled between the true data output terminal and the complement data output terminal of the storage element.

3. The ripple counter circuit of Claim 1, wherein the ripple counter circuit comprises an up counter, and the initialization terminals of the first storage element and the additional storage elements are reset terminals.

4. The ripple counter circuit of Claim 1, wherein the ripple counter circuit comprises a down counter, and the initialization terminals of the first storage element and the additional storage elements are set terminals.

5. The ripple counter circuit of Claim 1, wherein the control circuit comprises:

a second storage element having a data input terminal, a data output terminal, and a clock input terminal coupled to the clock input terminal of the ripple counter circuit; and

an inverting logic gate having a first input terminal coupled to the data output terminal of the second storage element, a second input terminal coupled to the test enable input terminal, and an output terminal coupled to the data input terminal of the second storage element and further coupled to the control output terminal of the control circuit.

6. The ripple counter circuit of Claim 5, further comprising an inverter coupled between the clock input terminal of the ripple counter circuit and the clock input terminal of the second storage element.

7. The ripple counter circuit of Claim 7, wherein the inverting logic gate comprises a logical NOR gate.

8. The ripple counter circuit of Claim 5, wherein the second storage element comprises a D-type flip-flop.

9. The ripple counter circuit of Claim 1, further comprising:

an oscillator having an output terminal; and

a clock select multiplexer having a first input terminal coupled to the clock input terminal of the ripple counter circuit, a second input terminal coupled to the output terminal of the oscillator, a select terminal coupled to the test enable input terminal of the control circuit, and an output terminal coupled to the clock terminal of the first storage element.

10. The ripple counter circuit of Claim 9, wherein the oscillator comprises a ring oscillator.

11. The ripple counter circuit of Claim 1, wherein the control circuit comprises an initialization terminal coupled to the initialization terminals of the first storage element and the additional storage elements.

12. The ripple counter circuit of Claim 11, wherein the ripple counter circuit further comprises an initialization circuit having an initialization output terminal coupled to the initialization terminals of the first storage element, the additional storage elements, and the control circuit.

13. The ripple counter circuit of Claim 12, wherein the initialization output terminal of the initialization circuit comprises a reset output terminal.

14. The ripple counter circuit of Claim 12, wherein the ripple counter circuit further comprises an initialization input terminal, the initialization circuit comprising:

a delay element having an input terminal and an output terminal; and

an initialization multiplexer having a first input terminal coupled to the initialization input terminal of the ripple counter circuit, a second input terminal coupled to the output terminal of the delay element, a select terminal coupled to the test enable input terminal of the control circuit, and an output terminal coupled to the initialization output terminal of the initialization circuit.

15. The ripple counter circuit of Claim 14, wherein the delay element comprises a plurality of flip-flops coupled in series, a first flip-flop of the series having a data input terminal coupled to ground and a last flip-flop of the series having a data output terminal coupled to the output terminal of the delay element.

16. The ripple counter circuit of Claim 14, wherein the delay element comprises a plurality of inverting logic gates coupled in series.

17. A method of testing a ripple counter circuit, comprising:

selecting a test mode of operation for the ripple counter circuit;

initializing the ripple counter circuit to store an initialization value;

automatically controlling the ripple counter circuit to enter a first state when in the test mode;

toggling, in the first state, each bit stored in the ripple counter circuit to provide a new stored value;

automatically controlling the ripple counter circuit to enter a second state when in the test mode; and

counting, in the second state, in response to a first edge on a clock input signal, wherein the ripple counter circuit stores a new value the same as the initialization value.

18. The method of Claim 17, wherein the first edge on the clock input signal is a rising edge.

19. The method of Claim 17, wherein toggling each bit stored in the ripple counter circuit comprises toggling the bits on receipt of another first edge on the clock input signal.

20. The method of Claim 17, wherein selecting a test mode of operation comprises providing a value on a test enable input signal, and automatically controlling the ripple counter circuit to enter a second state comprises overriding the value on the test enable input signal.

21. The method of Claim 17, wherein the initialization value is an all zeros value, the new stored value is an all ones value, and counting in response to a first edge on a clock input signal comprises adding one to the new stored value.

22. The method of Claim 17, wherein the initialization value is an all ones value, the new stored value is an all zeros value, and counting in response to a first edge on a clock input signal comprises subtracting one from the new stored value.

23. A ripple counter circuit, comprising:

means for selecting a test mode of operation for the ripple counter circuit;

means for initializing the ripple counter circuit to store an initialization value;

means for controlling the ripple counter circuit to automatically enter a first state followed by a second state when in the test mode;

means for toggling, in the first state, each bit stored in the ripple counter circuit to provide a new stored value; and

means for counting, in the second state, in response to a first edge on a clock input signal, wherein the ripple counter circuit stores a new value the same as the initialization value.

24. The ripple counter circuit of Claim 23, wherein the first edge on the clock input signal is a rising edge.

25. The ripple counter circuit of Claim 23, wherein the means for toggling each bit stored in the ripple counter circuit comprises means for toggling the bits on receipt of another first edge on the clock input signal.

26. The ripple counter circuit of Claim 23, wherein the means for selecting a test mode of operation comprises a test enable input signal, and the means for controlling the ripple counter circuit to automatically enter a first state followed by a second state comprises means for overriding the value on the test enable input signal when in the second state.

27. The ripple counter circuit of Claim 23, wherein the initialization value is an all zeros value, the new stored value is an all ones values, and the means for counting in response to a first edge on a clock input signal comprises means for adding one to the new stored value.

28. The ripple counter circuit of Claim 23, wherein the initialization value is an all ones value, the new stored value is an all zeros value, and the means for counting in response to a first edge on a clock input signal comprises means for subtracting one from the new stored value.